METHOD OF FABRICATING COMPLEMENTARY BIPOLAR TRANSISTORS WITH SiGe BASE REGIONS

FIELD OF THE INVENTION

[0001] The invention relates to a method of fabricating complementary bipolar transistors with SiGe base regions in an SiGe-BiCMOS process.

BACKGROUND OF THE INVENTION

[0002] Submicron structuring in advanced semiconductor processes achieves a high integration density. Submicron structuring by means of advanced lithographic techniques permits fabrication of greatly scaled down CMOS transistors. The achievable bandwidth and the available driver capacity is, however, restricted in CMOS processes. It is particularly for analog circuits requiring a high cutoff frequency that bipolar transistors are preferably employed, fabricated, for example, from gallium arsenide. Gallium arsenide transistors do not permit integration, however, in conventional CMOS processes. This is why more recently process technologies have been developed comprising fast bipolar transistors combinable with advanced CMOS technologies. One of these technologies is the SiGe-BiCMOS technology in which the base connections of the bipolar transistors are formed by a layer of silicon-germanium (SiGe). By injecting atoms of germanium into the base layers of the SiGe transistors the band gap energy is reduced so that these transistors feature substantially higher cutoff frequencies than transistors fabricated by a conventional bipolar method or BiCMOS method.

[0003] Injecting atoms of germanium into the base layers of bipolar transistors is the key to enhanced performance of these transistors. The silicon-germanium base layer is usually deposited by epitaxy.

[0004] Complementary transistors are often used in circuitry for implementing specific analog functions. Simultaneous epitaxial growth of the base layers of both transistors (NPN and PNP) does not permit optimizing the germanium

profile, however. For as high a cutoff frequency as possible PNP transistors and NPN transistors require differing germanium profiles.

SUMMARY OF THE INVENTION

[0005] The invention is thus based on the objective of providing a method with which the base layers of complementary bipolar transistors can be formed with an optimized germanium profile in a simple manner.

[0006] This objective is achieved with the inventive method of fabricating complementary bipolar transistors with SiGe base regions by forming on a wafer a first collector region and a second collector region juxtaposed and each comprising an epitaxial layer of silicon and depositing a layer of silicon enhanced with germanium crystalline over each collector region in steps each separate from the other so that crystalline SiGe layers of differing germanium profiles materialize over the collector regions.

[0007] This novel method in accordance with the invention now makes it possible to fabricate the base layers for complementary bipolar transistors in SiGe technology by the base layers being formed one after the other so that each complementary bipolar transistor can be fabricated for optimized performance of the base regions.

[0008] Advantageous further embodiments of the invention read from the sub-claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The invention will now be detailed with reference to the drawing in which:

[0010] Figs. 1a to 1f are section views depicting the steps in the method in accordance with the invention ; and

[0011] Fig. 2 is a section view through a precision resistor resulting from the method in accordance with the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0012] Referring now to Fig. 1a there is illustrated in a side view a section through a wafer 10 consisting substantially of silicon. Deposited on the wafer 10 are a few structures serving as the starting point for the method in accordance with the invention as detailed in the following. The wafer 10 comprises, running parallel to the top face, a buried layer 12 consisting of silicon dioxide, for example, and used for electrically insulating the overlying layers. Over the buried layer 12 the wafer 10 is provided with two regions formed simultaneously, each of which may form the collector region of a bipolar transistor. In the following the method in accordance with the invention is described for the case that in the left-hand region, termed PNP in Fig. 1a, a bipolar PNP transistor is to be formed whilst in the right-hand region termed NPN in Fig. 1a, a bipolar NPN transistor is formed.

[0013] In the first collector region the collector of an NPN transistor is formed. This region is termed in the following npn collector region 20. The npn collector region 20 consists of an epitaxial crystalline layer of silicon. The npn collector region 20 may be deposited over a so-called buried n-layer 22 interposed between the npn collector region 20 and the layer 12. The buried n-layer 22 consists of silicon doped with a high concentration of n-type dopant (for example arsenic or phosphor). The n-layer 22 serves to make available a low impedance contact to the npn collector region 20. For this purpose, a contact terminal 24 is provided which can produce a microconnection to the top face. The contact terminal 24 substantially consists of silicon doped with a high concentration of n-type dopant.

[0014] In the second collector region the collector of a PNP transistor is formed. This collector region is termed pnp collector region 14 in the following. The pnp collector region 14 for the PNP transistor consists of epitaxial crystalline silicon.

The pnp collector region 14 may be deposited over a buried p-layer 16 interposed between the pnp collector region 14 and the layer 12. The buried p-layer 16 consists of silicon doped with a high concentration of a p-type dopant (for example boron). The p-layer 16 serves to make available a low impedance contact to the pnp collector region 14. For this purpose a further contact terminal 18 is provided which can produce a microconnection to the top face. The further contact terminal 18 substantially consists of silicon doped with a high concentration of a p-type dopant.

[0015] Each of the inactive regions outside of the pnp collector region 14 with the buried p-layer 16 and outside of the npn collector region 20 with the buried n-layer 22 is provided with a trench 26 extending up to the layer 12. This trench 26 is filled with a dielectric such as silicon dioxide, silicon nitride or undoped polycrystalline silicon so that a planar surface is formed on the top face of the wafer.

[0016] Referring now to Fig. 1b there is illustrated how in a first step of the method in accordance with the invention an e.g. 12 nm thick layer of silicon dioxide 28 is deposited on the top face of the wafer 10. Deposited over the layer of silicon dioxide 28 is an e.g. 125 nm thick polycrystalline layer of silicon 30 provided with a photoresist. A first region comprising the npn collector region 20 and a small rim surrounding the npn collector region 20 is released of the polycrystalline layer of silicon 30 by photolithography and e.g. by means of a reactive ion etch technique to expose the layer of silicon dioxide 28, after which, by means of an etching process e.g. wet or dry, the exposed layer of silicon dioxide 28 is removed. The photoresist is subsequently totally removed.

[0017] Referring now to Fig. 1c there is illustrated how in the next step an e.g. 190 nm thick epitaxial layer of silicon is deposited on the top face of the wafer 10. During crystalline deposition germanium is added to the silicon and doped with a p-type dopant to thus form over the npn collector region 20 a crystalline layer of

SiGe 32a whilst over the polycrystalline layer of silicon 30 a polycrystalline layer of SiGe 32b is formed.

[0018] After this, an etch stop 34 is deposited on the top face of the wafer 10, the etch stop 34 consisting of a roughly 30 nm thick layer of silicon dioxide, for example.

[0019] Referring now to Fig. 1d there is illustrated how in the next step a photoresist is deposited on the top face of the wafer 10. A second region comprising the pnp collector region 14 and a small rim surrounding the pnp collector region 14 is released of etch stop 34, the polycrystalline layer of SiGe 32b and polycrystalline layer of silicon 30 by photolithography and by means of an etching technique to expose the layer of silicon dioxide 28, after which the photoresist is totally removed. With an etching process, e.g. wet or dry etching, the layer of silicon dioxide 28 is subsequently removed.

[0020] Referring now to Fig. 1e there is illustrated how in the following step a further epitaxial layer of silicon is deposited on the top face of the wafer 10, e.g. 190 nm thick. During crystalline deposition germanium is added to the further layer of silicon and doped with an n-type dopant to thus form over the pnp collector region 14 a further layer of crystalline SiGe 36a, whilst over the polycrystalline layer of silicon 30 a further layer of polycrystalline SiGe 36b is formed.

[0021] After this a resist 38 is deposited on the top face of the wafer 10. The resist 38 having a thickness of e.g. 15 nm may consist of silicon dioxide, formed, for example, by decomposition of tetraethylorthosilicate (TEOS).

[0022] The further layer of crystalline SiGe 36a and further layer of polycrystalline SiGe 36b may already be doped with an n-type dopant during crystalline deposition, although it is just as possible to implement n-doping, for example with

arsenic, not until after crystalline deposition by ion implantation. This may be implemented in several stages so that various regions of the further layer of crystalline SiGe 36a can be doped differingly in thickness to thus permit influencing the doping profile in the further layer of crystalline SiGe 36a.

[0023] Referring now to Fig. 1f there is illustrated how in the next step with the exception of the surface area over the pnp collector region 14 the resist 38 is totally removed. After this, a photoresist is deposited over the further layer of polycrystalline SiGe 36b and further layer of crystalline SiGe 36a, the photoresist being structured by photolithography. This is followed by the further layer of polycrystalline SiGe 36b, not protected by the photoresist, being removed, leaving the further layer of crystalline SiGe 36a over the pnp collector region 14 in place. By suitably submicron structuring the photoresist surrounding the further layer of crystalline SiGe 36a, the further layer of polycrystalline SiGe 36b is not removed. This remaining region of the further layer of polycrystalline SiGe 36b can be made use of in subsequent steps in processing for contacting the further layer of crystalline SiGe 36a forming the base region of the PNP transistor.

[0024] In subsequent steps in processing the etch stop 34 and polycrystalline layer of SiGe 32b can be removed by photolithography and etching, here too, similar to that as already described in the previous paragraph, the polycrystalline layer of SiGe 32b remaining in a microregion surrounding the polycrystalline layer of SiGe 32b for contacting the crystalline layer of SiGe 32a forming the base region of the NPN transistor.

[0025] Over the collector regions 20 and 14 the crystalline layers of SiGe 32a and 36a are formed in sequence by the method in accordance with the invention to form the base layers of bipolar transistors. Since the crystalline layers of SiGe 32a and 36a are each produced independently of the other, the profile of the germanium deposited in the silicon layer can be optimized for NPN and PNP

transistors. Thus, e.g. the base layer of the PNP transistor may be produced with a trapezoidal germanium profile whilst the base layer of the NPN transistor features a triangular germanium profile. The transistors fabricated by the method in accordance with the invention having optimized germanium profiles of the base layers excel by enhanced performance, such as more particularly elevated cutoff frequencies.

[0026] Applying the etch stop 34 in the method in accordance with the invention also permits fabrication of precision resistors. The polycrystalline layer of SiGe 32b underlying the etch stop 34 remains outside of the p-type collector region 14 during removal of the further layer of polycrystalline SiGe 36b since it is protected by the etch stop 34. Referring now to Fig. 2 there is illustrated a resistor located in a region outside of the active components (NPN and PNP transistors as well as CMOS structures produced by a different method) and formed by an implanted region of the polycrystalline layer of SiGe 32b and polycrystalline layer of silicon 30. The polycrystalline layer of SiGe 32b is covered by the etch stop 34. This layer is also used as a resist during implantation of the precision resistor.